GRID CONNECTED PV SYSTEM: Use of Single phase Inverter

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Abstract

This paper presents a single-phase five-level photovoltaic (PV) inverter topology for grid-connected PV systems with a novel pulsewidth-modulated (PWM) control scheme. Two reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switches. A digital PID control algorithm is implemented in Microcontroller to keep the current injected into the grid sinusoidal and to have high dynamic performance with rapidly changing atmospheric conditions. The inverter offers much less total harmonic distortionand can operate at near-unity power factor. The proposed system is verified through simulation and is implemented in a prototype, and the experimental results are compared with that with the conventional single-phase three-level grid-connected PWM inverter.

Index Terms— grid connected, photovoltaic (PV), proportional–integral (PI) current control, pulse width modulated (PWM) inverter.

I. INTRODUCTION

The demand for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to advancement in power electronics techniques. Photovoltaic (PV) sources are used today in many applications as they have the advantages of being maintenance and pollution free. Solar-electric-energy demand has grown consistently by 20%–25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices. This decline has been driven by the following factors:

1) An increasing efficiency of solar cells;
2) Manufacturing technology improvements; and
3) Economies of scale [1]. PV inverter,

Which is the heart of a PV system, is used to convert dc power obtained from PV modules into ac power to be fed into the grid. Improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation of the inverter [2]. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional

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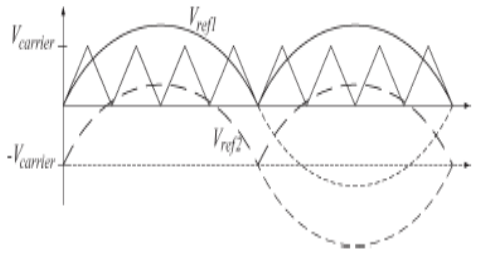
three-level pulse width-modulated (PWM) inverters.

They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD), and others .The three common topologies for multi level inverters are asfollows:

1) diode clamped (neutral clamped
2) capacitor clamped (flying capacitors)
3) cascaded H-bridge inverter

In addition, several modulation and control strategies have been developed or adopted for multilevel inverters, including the following: multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and spacevector modulation A typical single-phase three-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following three values: zero, positive (+Vdc), and negative (−Vdc) supply dc voltage (assuming that Vdc is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions.Therefore, their harmonic reduction is limited to a certain degree [4].To overcome this limitation, this paper presents a five-level PWM inverter whose output voltage can be represented in the following five levels: zero, +1/2Vdc, Vdc, −1/2Vdc, and −Vdc. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. Both the reference signals *V*ref1 and *V*ref2 are identical to each other, except for an offset value equivalent to the amplitude of the carrier signal *V*carrier, as shown in Fig. 1.



Ease of Use: The inverter is used in a PV system, a proportional– integral (PI) current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity. Simulation and experimental results are presented to validate the proposed inverter configuration.

II. FIVE-LEVEL INVERTER TOPOLOGY AND PWM LAW

The proposed single-phase five-level inverter topology is shown in Fig. 2. The inverter adopts a full-bridge configuration with an auxiliary circuit [4]. PV arrays are connected to the inverter via a dc–dc boost converter. Because the proposed inverter is used in a grid-connected PV system, utility grid is used instead of load. The dc–dc boost converter is used

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to step up inverter output voltage *V*inv to be more than √2 of grid voltage *Vg* to ensure power flow from the PV arrays into the grid [19]. A filtering inductance *Lf* is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal PWM is used because it is one of the most effective methods. Sinusoidal PWM is obtained by comparing a high-frequency carrier with a low-frequency sinusoid, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency.

The switching instant is determined from the crossing of the carrier and the modulating signal. *A. Sinusoidal PWM Law* A fundamental period in Fig. 3 consists of *p* pulses whose widths vary sinusoidally throughout the cycle to give the fundamental component of frequency. The basis of equivalence between the desired sinusoid and the actual pulsed waveform is taken to be volt–seconds, as shown in Fig. 3, i.e., *As*1 = *Ap*1 and *As*2 = *Ap*2. One of these pulses, the general *k*th pulse, is chara

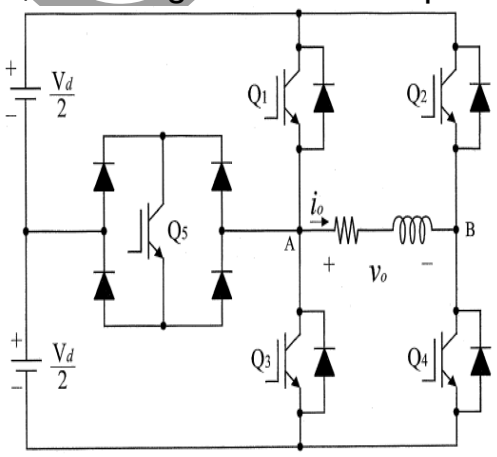

Figure 2 Configuration of the proposed single-phase five-level PWM inverter**.**

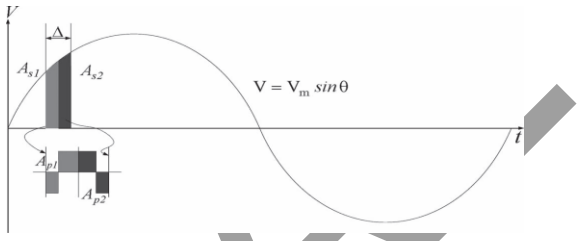

Fig. 3. Basis of equivalence for sinusoidal PWM

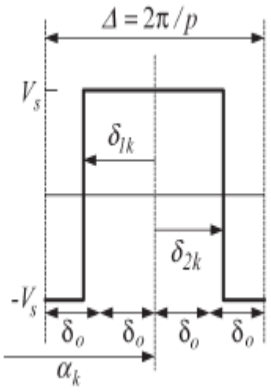

Fig. 4. Characterization of pulse.

The switching period Δ and the frequency modulation ratio *p* are, respectively, given by

Δ =2*π/p* (1)

p =*fs/f*1 (2)

where *fs* is the switching frequency and *f*1 is the fundamental frequency. The quarter period of pulse *δ*0 is given as

*δ*0 = Δ/4. (3)

αk is the position from the origin of the fundamental period of the midpoint of the period Δ. The angles *δ*1*k* and *δ*2*k* are the modulating angles which vary throughout the cycle, and it is to

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calculate these angles that a modulation law must be derived.
Consider first the average voltages $V1k$ and $V2k$ during the two halves of the modulating pulse

$$V1k = (Vs)\{\delta 1k - (2\delta 0 - \delta 1k)\}/2\delta 0 \quad (4)$$
$$\therefore V1k = (Vs)(\delta 1k - \delta 0)/\delta 0 \quad (5)$$
$$= (Vs)\beta 1k \quad (6)$$
where $1k = (\delta 1k - \delta 0)/\delta 0 \quad (7)$
and, similarly

$$V2k = (Vs)\beta 2k \quad (8)$$
Where

$$\beta 2k = (\delta 2k - \delta 0)/\delta 0. \quad (9)$$

The volt–second $As1$ is the half-pulsewidth of the sine wave and is given according to Fig. 4 by
$$As1 = \alpha k f$$
$$\alpha k - 2\delta 0$$
$$Vm \sin\theta \, d\theta \quad (10)$$
$$= 2Vm \sin\delta 0 \sin(\alpha k - \delta 0). \quad (11)$$
However, $\sin\delta 0 \rightarrow \delta 0$ when $\delta 0$ is small
$$\therefore As1 = 2\delta 0 Vm \sin(\alpha k - \delta 0) \quad (12)$$
and, similarly,
$$As2 = 2\delta 0 Vm \sin(\alpha k + \delta 0). \quad (13)$$
For the corresponding volt–second $Ap1$, in thePWMwaveform,
$$Ap1 = 2\delta 0 V1k \quad (14)$$
$$\therefore Ap1 = 2\delta 0 \beta 1k (Vs) \quad (15)$$
and, similarly,
$$Ap2 = 2\delta 0 \beta 2k (Vs). \quad (16)$$
For equivalence of volt–seconds from which the modulation law can be derived, we require that
$$As1 = Ap1 \quad (17)$$
$$As2 = Ap2. \quad (18)$$

By equating (12) and (14), and (13) and (16)
$$\beta 1k = M \sin(\alpha k - \delta 0) \quad (19)$$
and, similarly,
$$\beta 2k = M \sin(\alpha k + \delta 0) \quad (20)$$

where M is the "modulation index" and
$$M = Vm/Vs. \quad (21)$$

Equation (21) can be expressed in terms of amplitude of carrier signal Vc by replacing Vs with Vc. Because, in this topology,two identical reference signals are used, $Vs = 2Vc$ and $Vm = V\text{ref}1 = V\text{ref}2$. If $M > 1$, higher harmonics in the phase waveform are obtained. Therefore, M is maintained between zero and one. If the amplitude of the reference signal is increased to be higher than the amplitude of the carrier signal, i.e., $M > 1$, this will lead to overmodulation. Large values of M in sinusoidal PWM techniques lead to full overmodulation [20]. Fig. 6 shows the carrier and reference signals for different values of M. Equations (19) and (20) define the modulation law, which is more M. (a)$M = 0.3$. (b)$M = 0.5$. (c)$M = 0.7$. (d)$M = 1.2$. commonly expressed in terms of $\delta 1k$ and $\delta 2k$, by substitutingfrom (7) and (9) to give

$$\delta 1k = \delta 0 \, [1 + M \sin(\alpha k - \delta 0)] \quad (22)$$

$$\delta 2k = \delta 0 \, [1 + M \sin(\alpha k + \delta 0)] \, . \quad (23)$$

Thus, the switching angles $\delta 1k$ and $\delta 2k$ for the kth pulse can be calculated from

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(22) and (23) in terms of modulation index *M* and angles *αk* and *δ*0 which depend upon the fundamental frequency and frequency ratio. *B. Harmonic Spectrum of* Sinusoidal PWM Waveform The voltage harmonics produced by the sinusoidal PWM can be computed by first calculating the harmonics due to the *k*th pulse alone, *Ank*, and then summating the harmonic contributions of all *p* pulses

Switches S_1–S_3 will be switching at the rate of the carrier signal frequency, where as S_4 and S_5 will operate at a frequency equivalent to the fundamental

S_1	S_2	S_3	S_4	S_5	V_{inv}
ON	OFF	OFF	OFF	ON	$+V_{pv}/2$
OFF	ON	OFF	OFF	ON	$+V_{pv}$
OFF	OFF or (ON)	OFF or (ON)	ON or (OFF)	ON or (OFF)	0
ON	OFF	OFF	ON	OFF	$-V_{pv}/2$
OFF	OFF	ON	ON	OFF	$-V_{pv}$

Table 1 Inverter Output Voltage during S_1−S_5 Switch on and off

frequency. Table 1 illustrates the level of *V*inv during S_1–S_5 switch on and off. Figure 5 shows Switching pattern for the single-phase five-level

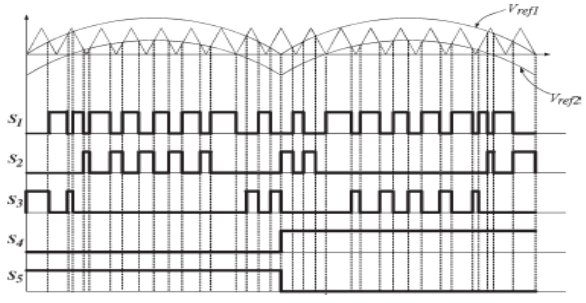

Figure 5 Switching pattern for the single-phase five-level inverter.

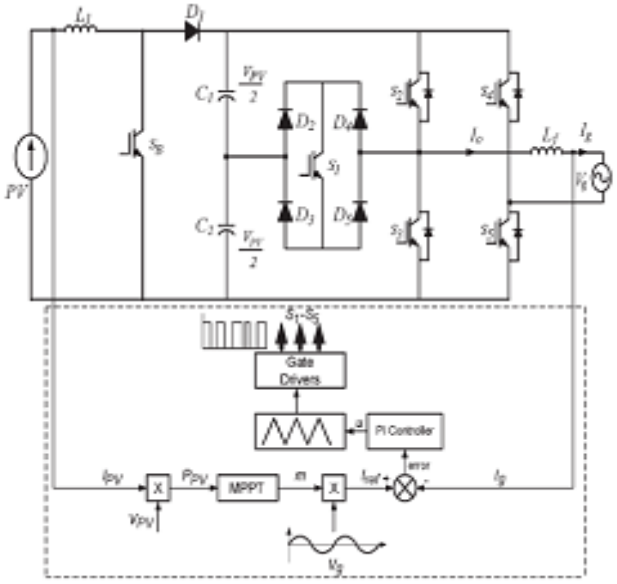

Figure 6 single-phase five-level inverter with PI controller**.**

The proposed single-phase five-level inverter topology is shown in Fig. 6. The inverter adopts a full-bridge configuration with an auxiliary circuit. PV arrays are connected to the inverter via a dc–dc boost converter. Because the proposed inverter is used in a grid-connected PV system, utility grid is used instead of load. The dc–dc boost converter is used to step up inverter output voltage *V*inv to be more than √2 of grid voltage *Vg* to ensure power flow from the PV arrays into the grid. A filtering inductance *Lf* is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal

PWM is used because it is one of the most effective methods. Sinusoidal PWM is obtained by comparing a high-frequency carrier with a low-frequency sinusoid, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency.The switching instant is determined from the crossing of the carrier and the modulating signal.

$$A_{nk} = \frac{1}{2\pi} \int_{\alpha_k - 2\delta_0}^{\alpha_k + 2\delta_0} V(\theta) e^{-jn\theta}\, d\theta \tag{24}$$

$$\therefore A_{nk} = \frac{1}{2\pi} \left\{ - \int_{\alpha_k - 2\delta_0}^{\alpha_k - \delta_{1k}} V_s e^{-jn\theta}\, d\theta + \int_{\alpha_k - \delta_{1k}}^{\alpha_k + \delta_{2k}} V_s e^{-jn\theta}\, d\theta - \int_{\alpha_k + \delta_{2k}}^{\alpha_k + 2\delta_0} V_s e^{-jn\theta}\, d\theta \right\} \tag{25}$$

$$= (V_s) \left(\frac{1}{2\pi}\right) \left(\frac{-2}{jn}\right) \times \{e^{-jn\delta_{2k}} - e^{jn\delta_{1k}} + j \sin 2n\delta_0\} e^{-jn\alpha_k}. \tag{26}$$

$$A_n = \sum_{k=1}^{p} A_{nk}. \tag{27}$$

$$u(t) = K_p e(t) + K_i \int_{\tau=0}^{\tilde{} } e(\tau) d\tau \tag{28}$$

u(*t*) control signal;
e(*t*) error signal;
t continuous-time-domain time variable;
τ calculus variable of integration;
Kp proportional-mode control gain;
Ki integral-mode control gain.
Implementing this algorithm using a PIC requires one to transform it into the discrete-time domain. Trapezoidal sum approximation is used to transform the integral term into the discrete-time domain because it is the most straightforward technique. The proportional term is directly used without approximation.

P term : *Kpe*(*t*) = *Kpe*(*k*). (29)

Time relationship: $t = k * h$
where
h sampling period;
k discrete-time index: *k* = 0, 1, 2, ...
For simplification, it is convenient to define new controller gains as

K_i = Ki h/2 (30)

from which one can construct the discrete-time PI control

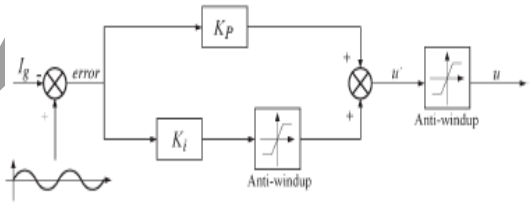

Fig. 7 PI control algorithm implemented in PIC controller.

$$\text{I term}: \quad K_i \int_{\tau=0}^{t} e(\tau) d\tau \cong K_i \sum_{i=0}^{k} \frac{h}{2} [e(i) + e(i-1)]. \tag{30}$$

$$K_i' = K_i \frac{h}{2} \tag{31}$$

$$u(k) = K_p e(t) + K_i' \sum_{}^{k} [e(i) + e(i-1)]. \tag{32}$$

$$\text{sum}(k) = \text{sum}(k-1) + [e(k) + e(k-1)] \tag{33}$$

$$u(k) = K_p e(k) + K_i' \text{sum}(k). \tag{34}$$

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B. ALGORITHM IMPLEMENTATION

Control signal saturation and integral-mode antiwindup limiting are easily implemented in software. In this work, the control signal itself takes the form of PWM outputs from the PIC. Therefore, the control signal is saturated at the value that corresponds to 100% duty cycle for the PWM. An undesirable side effect of saturating the controller output is the integral-mode windup. When the control output saturates, the integral-mode control term (i.e., the summation) will continue
to increase but will not produce a corresponding increase in controller output (and hence will not produce any additional increase in plant response). The integral can become quite large, and it can take a long time before the controller is able to reduce it once the error signal changes sign. The effects of windup

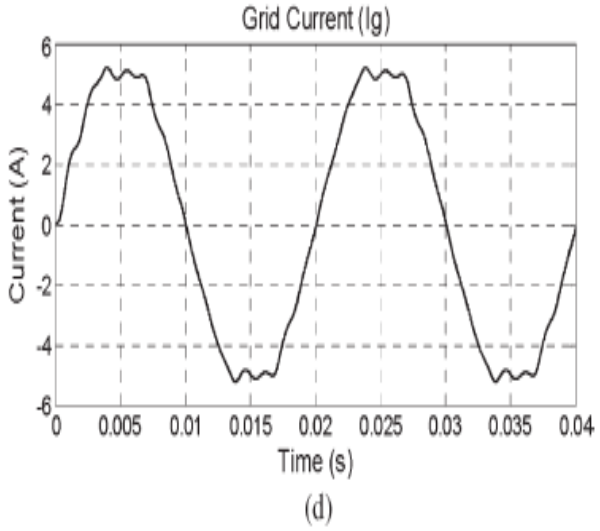

Fig. 7. Fig shows grid current of the circuit

V. SIMULATION RESULTS

Let us consider the following example, inverter circuit involving unipolar switching. It is connected with an R Load as shown below.

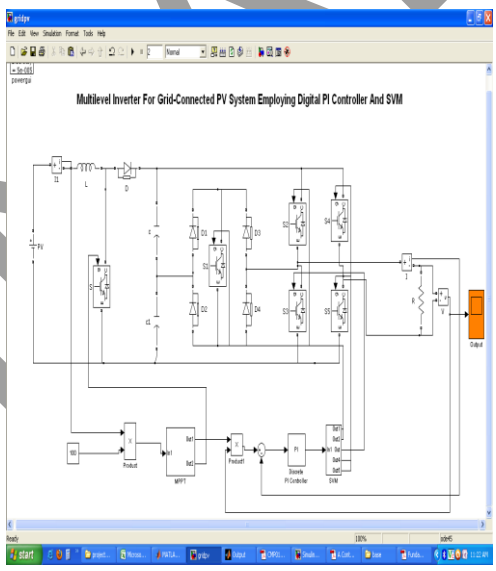

Figure 8 Simulation Circuit Diagram

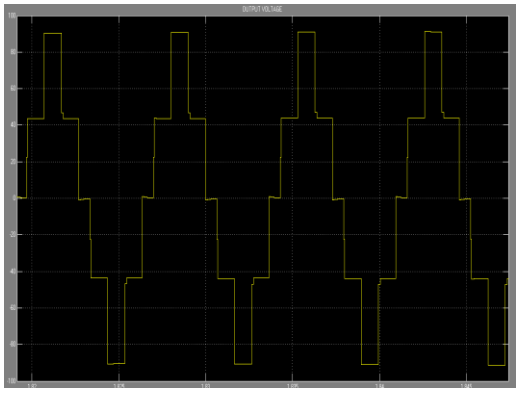

Figure 9 five level Output Waveform the inverter circuit

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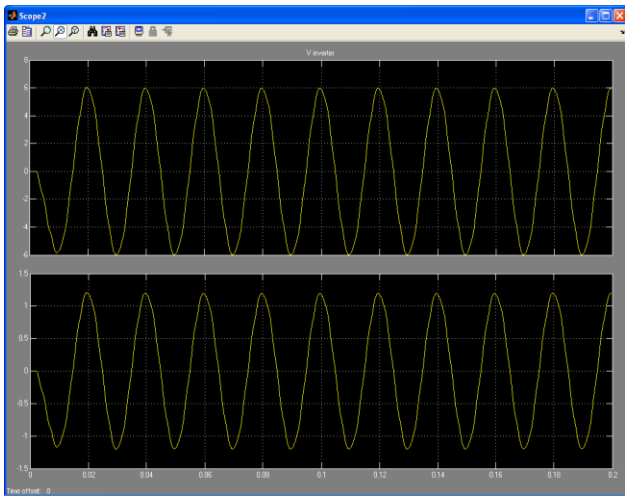

Figure 10 filtered Output Waveform from the inverter

In order to verify that the proposed inverter can be practically implemented in a PV system, simulations were performed by using MATLAB SIMULINK. It also helps to confirm the PWM switching strategy which then can be implemented in a PIC. It consists of two reference signals and a triangular carrier signal. Both the reference signals are compared with the triangular carrier signal to produce PWM switching signals for switches S_1−S_5. Note that one leg of the inverter is operating at a high switching rate equivalent to the frequency of the carrier signal, whereas the other leg is operating at the rate of fundamental frequency (i.e., 50 Hz).
Figure 8 shows the Simulation Circuit Diagram The tch at the auxiliary circuit S_1 also operates at the rate of the carrier signal. As mentioned earlier, the modulation index M will determine the shape of the inverter output voltage Vinv and the grid current Ig shows Vinv and Ig for different values of M. The dc-bus voltage is set at 400 V (>√2Vg) in this case, Vg is 240 V in order to inject current into the grid. Vinv is less than √2Vg due to M being less than 0.5.The inverter should not operate at this condition because the current will be injected from the grid into the inverter, rather than the PV system injecting the current into the grid. Figure 9 shows five level Output Waveform the inverter circuit and Figure 10 shows the five level output Waveform the inverter circuit.

VI .CONCLUSION

Improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation of the inverter. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level Pulse Width Modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD).

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